Revision Notes Class 12

Physics

Chapter 14 - Semiconductor Electronics

1. ENERGY BANDS IN SOLIDS

In case of solids, there are single energy levels where the atoms are arranged in a systematic space lattice and therefore the atom is highly influenced by the neighboring atoms for a single isolated atom. The closeness of atoms will be resulting in the intermixing of electrons of the neighboring atoms of course, for the valence electrons, not strongly bounded by the nucleus, in the outermost shells. Because of the intermixing the number of permissible energy levels will be increased or there will be significant variations in the energy levels. Therefore, instead of single energy levels related with the single atom in the case of a solid, there will be bands of energy levels.

1.1 Conduction Band, Valence Band & Forbidden Energy Gap

The band created by a series of energy levels including the valence electrons can be defined as valence band. The valence band can be explained as a band which is inhabited by the valence electrons or a band which is having highest inhabited band energy.The conduction band can be explained as the least unfilled energy band. The forbidden energy gap can be defined as the separation between conduction band and valence band. There will be no permitted energy state in this gap and therefore electron can’t occupy in the forbidden energy gap.

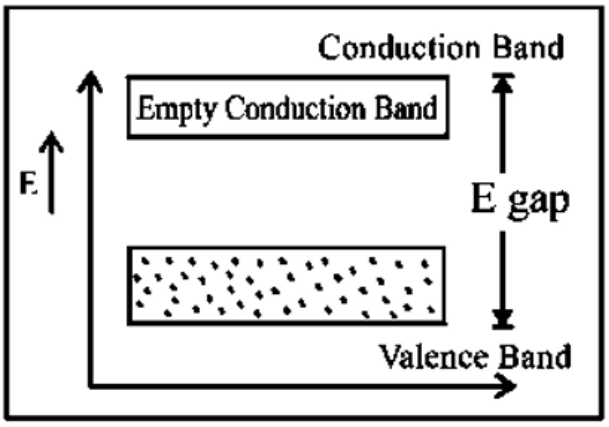
1.2 Conductors, Semiconductors and Insulators

Conductors are the materials which can conduct the charge carriers easily. Insulators are the materials in which the free flow of charge carriers is not possible. And semiconductors are the materials which is having conductivity in between insulators and conductors.According to the forbidden band, the insulators, semiconductors and conductors can be explained as mentioned below:

1.2.1 Insulators

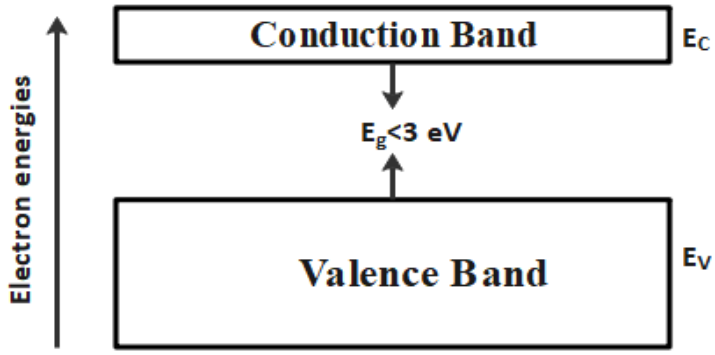
The forbidden energy band will be very wide in case of insulators. Because of this information electrons will not be jumped from valence band to conduction

band. The valence electrons will be bond very tightly to their parent atoms in insulators. Increase in temperature will be enabling some electrons to move to the conduction band.



1.2.2 Semiconductors

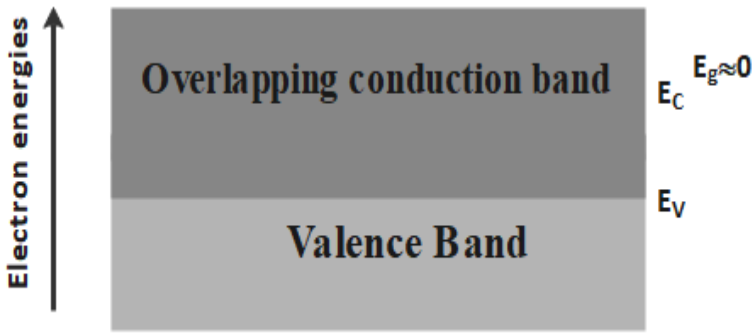
The forbidden band will be very small in semiconductors. Silicon and Germanium can be taken as the examples of semiconductors. A semiconductor material will be the one having electrical characteristics lying between insulators and good conductors. If a little amount of energy has been supplied, the electrons can jump from valence band to conduction band easily. As an example, if the temperature will be enhanced, then the forbidden band will be reduced such that some electrons are liberated into the conduction band.



1.2.3 Conductors

There will be no forbidden band and the valence band and conduction band overlap each other, in case of the conductors. Here a lot of free electrons will be available for the conduction of electricity. A small potential difference across the conductor will be causing the free electrons for including the electric

current. The very relevant point in conductors is that because of the absence of forbidden band, there will be no structure for establishing holes. The summation of current in conductors will be simply a flow of electrons.



2. SEMICONDUCTORS

Hence, semiconductor can be defined as a substance which is having resistivity in between conductors and insulators.

Semiconductors will be having the properties mentioned below.

(i) They will be having less resistivity than insulators and more than conductors.

(ii) The resistance of semiconductor will be reduced with the increase in temperature and vice versa.

(iii) If suitable metallic impurity such as arsenic, gallium etc. will be added to a semiconductors, its current conducting characteristics varies appreciably.

2.1 Impact of temperature of Semiconductors

The semiconductor crystal will be acting like a proper insulator since the covalent bonds are pretty much strong and no free electrons are available. At room temperature, some of the covalent bonds will be broken due to the thermal energy given to the crystal. Due to the breakage of the bonds, some electrons will be free which were inhabited in the production of these bonds.

The non-appearance of the electron in the covalent bond can be represented by a small circle. Therefore Hole can be shown as an empty place or vacancy left behind in the crystal structure. Since an electron is having unit negative charge, the hole will be similarly having a unit positive charge.

2.2 Mechanism of conduction of Electrons and Holes

If the electrons are released on the breakage of the covalent bonds, they will be moving randomly through the lattice of crystal.If an electric field has been applied, these free electrons will be having a uniform drift which is opposite to the direction of field applied. This can be referred as the electric current. If a covalent bond is broken, a hole has been produced. One hole is produced when one electron set free. This thermal energy will be producing electron-hole pairs-there will be as many holes as free electrons. These holes can go through the crystal lattice in a random fashion such as free electrons. The holes drift in the direction of applied field, if an external electric field is applied. Hence, this can be referred as electric current.

There will be a strong proneness of semiconductor crystal for producing a covalent bonds. Hence, a hole will be attracting an electron from the neighboring atom. Now a valence electron from nearby covalent bond will be coming for occupying in the hole at A. This will cause in a production of hole at B. The hole will be therefore successfully shifted from A to B. This hole will be moving from B to C from C to D and so on.

This movement of the hole in the non-appearance of an applied field will be random. But the hole gets drifted along the applied field, if an electric field has been applied.

2.3 Generation and Recombination of Carrier

The electrons and holes will be produced in pairs. The free electrons and holes will move within the crystal lattice in an irregular manner. There is always a chance that an electron which is free will be meeting with a hole, in such a random motion. If a free electron encounter a hole, they will recombine for re-establishing the covalent bond. Both the free electron and hole will be destroyed in the process of recombination and cause in the emission of energy as heat. The energy produced thereby, may in turn will get re-absorbed by another electron for breaking its covalent bond. In this manner a new electron-hole pair will be generated.

Hence, the method of splitting of covalent bonds and recombination of electrons and holes will be taking place simultaneously. If the temperature will be increased, the rate of generation of electrons and holes will be enhanced. This is turn increases, the densities of electrons and hole will get increased. Because of this the conductivity of semiconductor will be increased or

resistivity decreased. This will be the reason that semiconductors is having negative temperature coefficient of resistance.

2.4 Pure or Intrinsic Semiconductor and Impure or Extrinsic Semiconductors

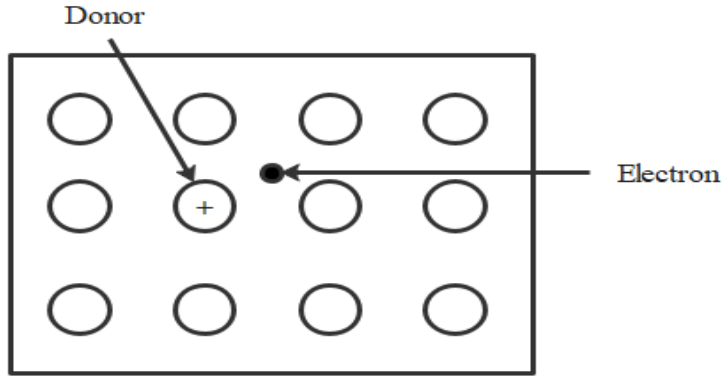
Intrinsic semiconductor can be defined as a semiconductor in which electrons and holes are solely produced by thermal excitation or a semiconductor in an extremely pure form is referred as a pure or intrinsic semiconductor. The number of free electrons will be always equivalent to the number of holes in intrinsic semiconductor.

2.4.1 Extrinsic Semiconductors

The electrical conductivity of intrinsic semiconductor will be enhanced by the addition of some impurity in the method of crystallization. The added impurity will be very small of the order of one atom per million atoms of the pure semiconductor. This kind of semiconductor can be referred as impurity or extrinsic semiconductor. The method of infusing impurity to a semiconductor can be defined as doping.The doping material will be either pentavalent atoms such as bismuth, antimony, arsenic, phosphorus which are having five valence electrons or trivalent atoms such as gallium, indium, aluminium, boron which are having three valence electrons. The pentavalent doping atom can be referred as donor atom since it is donating one electron to the conduction band of pure semiconductor. The doping materials can be referred as impurities as they change the structure of semiconductor crystals which are pure.

2.4.2 N–Type Extrinsic Semiconductor

If a little amount of pentavalent impurity has been added to a pure semiconductor crystal while the crystal growth, the produced crystal can be referred as N-type ext1rinsic semiconductor.



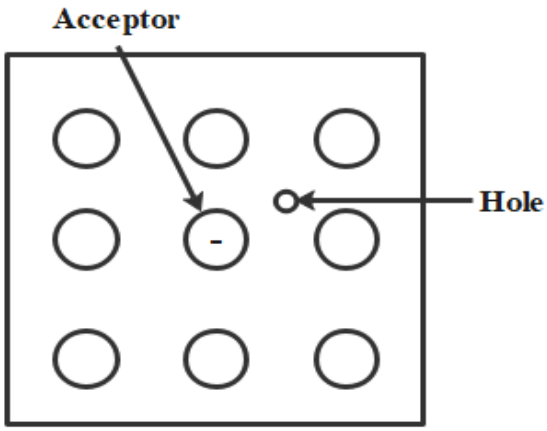
The following points should be remembered in case of N-type semiconductor

(i) The electrons will be the majority carriers while positive holes are minority carriers, in N-type semiconductor.

(ii) Even though N-type semiconductor is having excess of electrons but it will be electrically neutral. This will be because of the fact that electrons are produced by the addition of neutral pentavalent impurity atoms to the semiconductor. That is, there will be no addition of either positive or negative charges.

2.4.3 P–Type Extrinsic Semiconductor

If a little amount of trivalent impurity has been added to a pure crystal while the crystal growth, the produced crystal can be referred as P-type extrinsic semiconductor.



The following points should be remembered in case of P-type semiconductor:

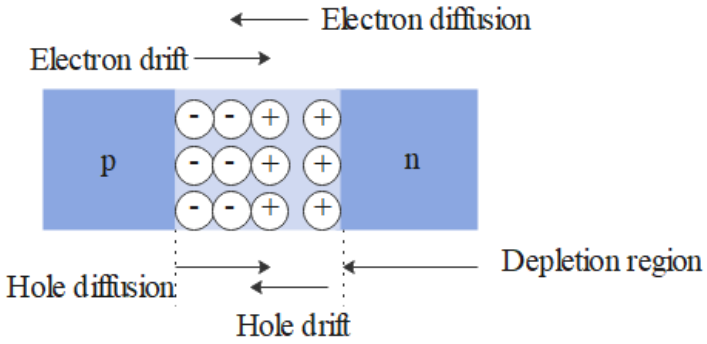
(i) The majority carriers are positive holes but minority carriers are the electrons in P-type semiconductor materials.

(ii) The P–type semiconductor will be remaining electrically neutral as the number of mobile holes under all conditions remains equivalent to the number of acceptors.

2.5 P–N Junction Diode

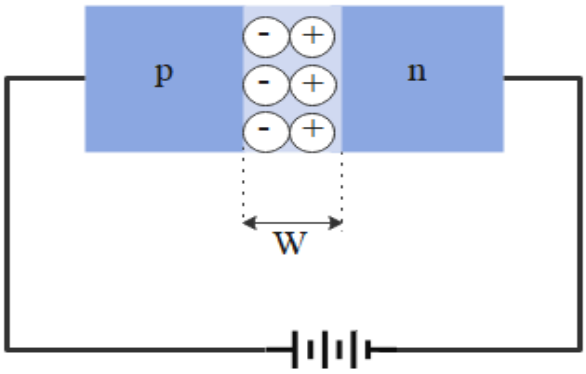
If a P-type material has joined to N-type intimately, a P-N junction will be created. Joining the two pieces a P-N junction will not be formed due to the surface films and other irregularities create major discontinuity in the crystal structure. Hence, a P-N junction will be created from a piece of semiconductor (say, germanium) by diffusing P-type material to one half side and N-type material to other half side. If P-type crystal has kept in contact with N-type

crystal so as to produce one piece, the assembly so required will be defined as P-N junction diode.



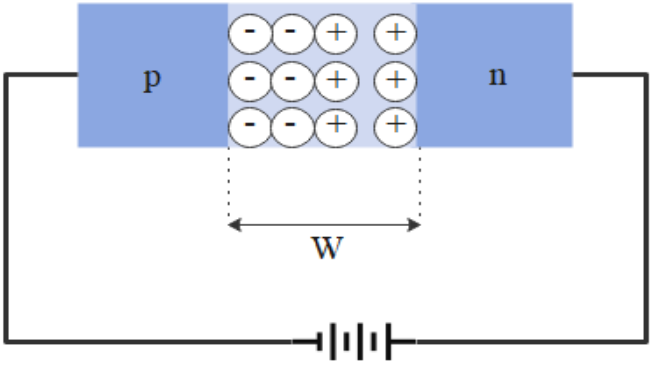
2.5.1 Forward Bias

The junction diode can be defined as forward biased, if external d.c. source has been connected to the diode with p–section connected to positive pole and n–section connected to negative pole.

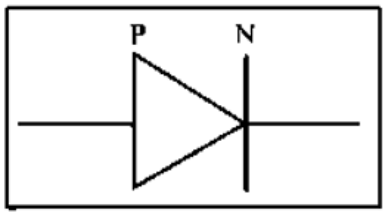


2.5.2 Reverse Bias

The junction diode can be defined as reverse biased, if an external d.c. battery has been connected to junction diode with P–section connected to negative pole and n–section connected to positive pole.



NOTE:
P–N JUNCTION can be defined as a device which will be offering low resistance when forward biased and act as an insulator if reverse biased.
Symbol:



2.6 Junction Diode as Rectifier

An electronic device which will be transforming a.c. power into d.c. power can be defined as a rectifier.

2.6.1 Principle

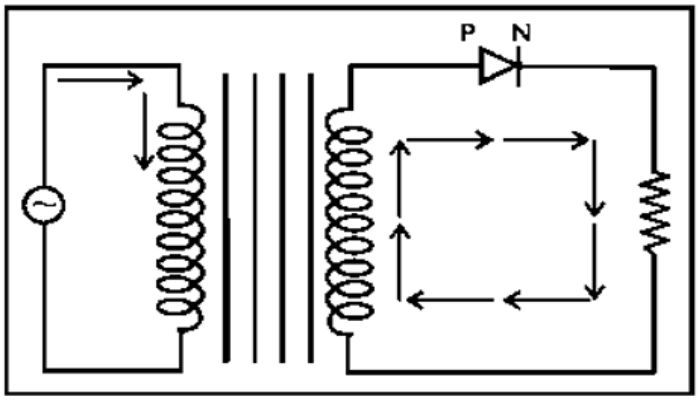
If forward biased, Junction diode will be offering a low resistive path and high resistance if reverse biased.

2.6.2 Arrangement

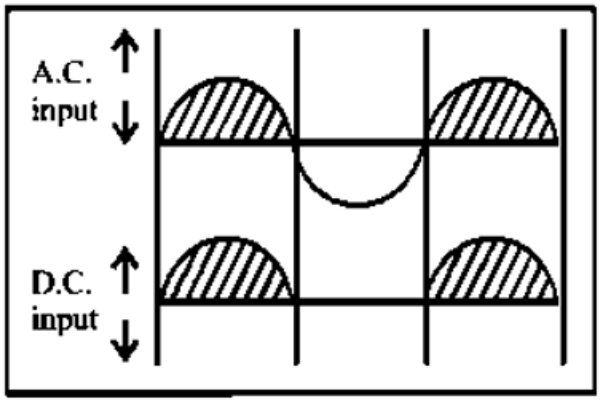
The a.c. supply will be given across the primary coil (P) of step down transformer. The secondary coil 'S' of transformer will be in connection to the junction diode and load resistance R_L. The output d.c. voltage will be received across R_L.

2.6.3 Theory

Assume that when first half of a.c. input cycle occurs, the junction diode will be forward biased. The conventional current will be flowing in the direction of arrow heats.



The upper end of R_L will be at positive potential with respect to the lower end. The magnitude of output across R_L while first half at any moment will be proportional to magnitude of current through R_L, which in turn will be proportional to magnitude of the forward bias and which will be dependent upon the value of a.c. input at that time ultimately.



Hence, output across R_L will be changing with respect to a.c. input. While second half, junction diode will be getting reverse biased and therefore no–output will be there. Hence, a discontinuous supply will be received.

2.7 Full Wave Rectifier

A rectifier which will be rectifying both halves of a.c. input can be referred as full wave rectifier.

2.7.1 Principle

Junction Diode will be giving low resistive path if forward biased and high resistive path if reverse biased.

2.7.2 Arrangement

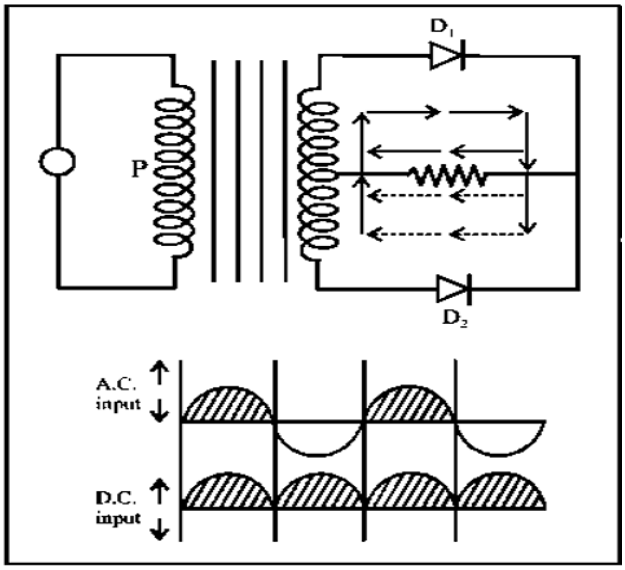
The a.c. supply has been supplied across the primary coil (P) of step down transformer. The two ends of S–coil (secondary) of transformer will be connected to P-section of junction diodes D_1 and D_2. A load resistance R_L will be connected across the n–sections of two diodes and central tapping of secondary coil. The d.c. output will be received across secondary.

2.7.3 Theory

Assume that while first half of input cycle upper end of s-coil will be at +ve potential. The junction diode D_1 will be getting forward biased, while D_2 will

be getting reverse biased. The conventional current because of D_1 will flow along path of full arrows.

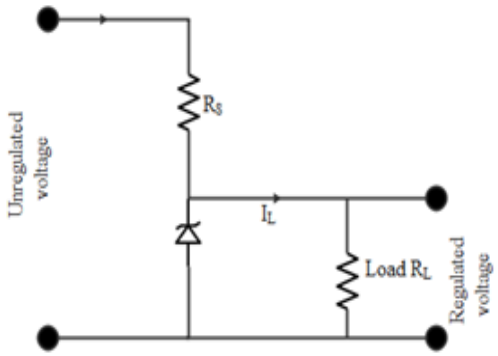
If second half of input cycle comes, the conditions will be in opposite manner. Now the junction diode D_2 will be conducting and the conventional current will be flowing along path of the dotted arrows. The output during both the half cycles will be of similar nature as the current during both the half cycles flows from right to left through load resistance R_L .The right end of R_L will be at +ve potential in accordance with left end. Hence, the output will be continuous in full wave rectifier.



Special usages of P-N junction diode:

a) Zener diode:

The zener diodes can be defined as a heavily doped P-N junction diode where the operation of the device can occur only in the reverse biased condition. Here as both p and n sides are heavily dope, the depletion region developed will be very thin. In this diodes, when the applied reverse bias voltage reaches the breakdown voltage of the zener diode, we can see a huge variation in the current. At this time, the reverse voltage will be almost a constant even though there is significant change in the current occurs. Hence this kind of diodes can

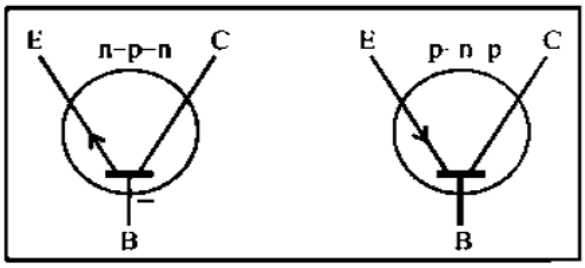


be used a voltage regulators. The above shown image is showing the Zener diode as a DC voltage regulator. Here we have to choose the Zener diode in accordance to the needed output voltage and the series resistance R_s accordingly.

2.8 Transistor

This will be a three section semiconductor, where three sections are combined so that the two at extreme ends will be having similar kind of majority carriers. At the same time, the section that is separating them will be having the majority carriers in opposite nature. The three sections of transistor can be defined as emitter (E), Base (B) and collector (C).

Symbol:



2.8.1 Action of n-p-n Transistor

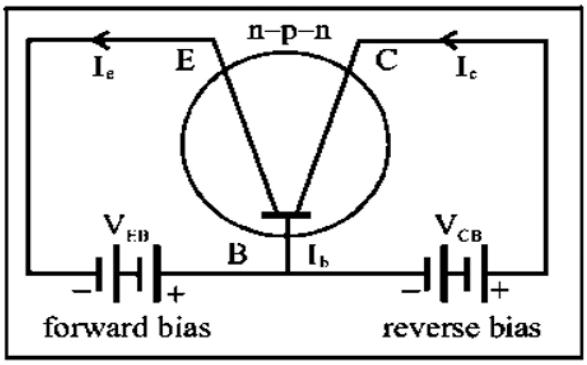


Fig. mentions that, the n-type emitter will be forward biased when connected it to $-$ve pole of V_{EB} (emitter-base battery) and n-type collector will be reverse biased when connected it to $+$ve pole of V_{CB} (collector-base battery).

The majority carriers (e^-) in emitter will be repelled towards base because of the forward bias. The base will be having holes as majority carriers but their number density is small because it is doped very lightly (5%) when we compare to emitter and collector. Because of the probability of e^- and hole combination in base will be small. Most of e^- (95%) cross into collector region where they will be swept away by $+$ve terminal of battery V_{CB}.

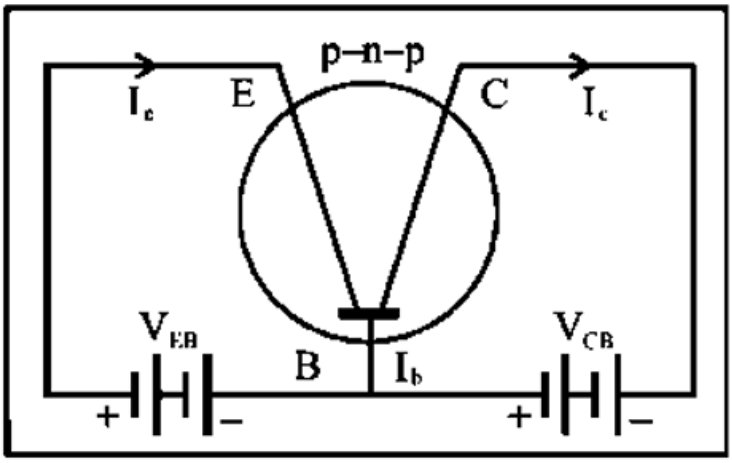
In corresponds to each electron that is taken by collector, an electron will enter the emitter from $-$ve pole of collector – base battery.

When I_e, I_b, I_c be emitter, base and collector current respectively then by the use of Kirchoff's first law, we can say that,

$I_e = I_b + I_c$

2.8.2 Action of p–n–p Transistor

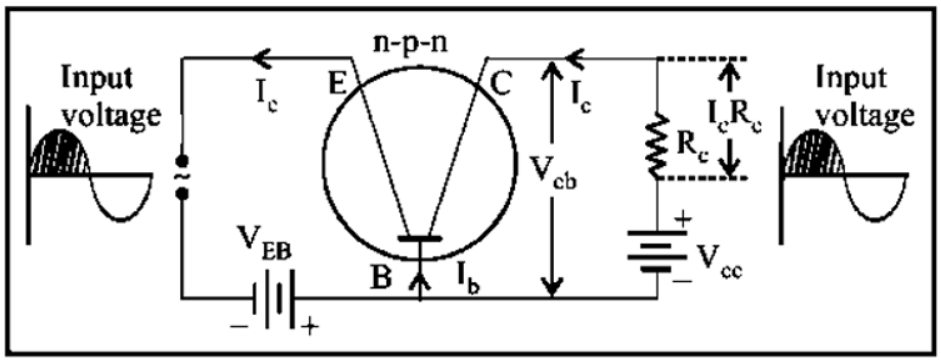
The p–type emitter will be forward biased when we connect it to $+$ve pole of emitter–base battery and p–type collector will be reverse biased when it is connected to $-$ve pole of collection - base battery. Here, majority carriers in emitter, that is holes will be repelled towards base because of forward bias. As base is lightly doped, it will be having low number density of e^-. If hole enters base region, then only 5% of e^- and hole combination will be occurring. Most of the holes will be reaching the collector and are swept away by $-$ve pole of V_{CB} battery.



2.9 Common base Amplifier

Here, base of the transistor will be common to both emitter and collector.

(a) Amplifier circuit **by the use of n-p-n transistor:** The emitter will be forward biased by the use of emitter bias battery (Vcc) and because of this, resistance of output circuit will be large.



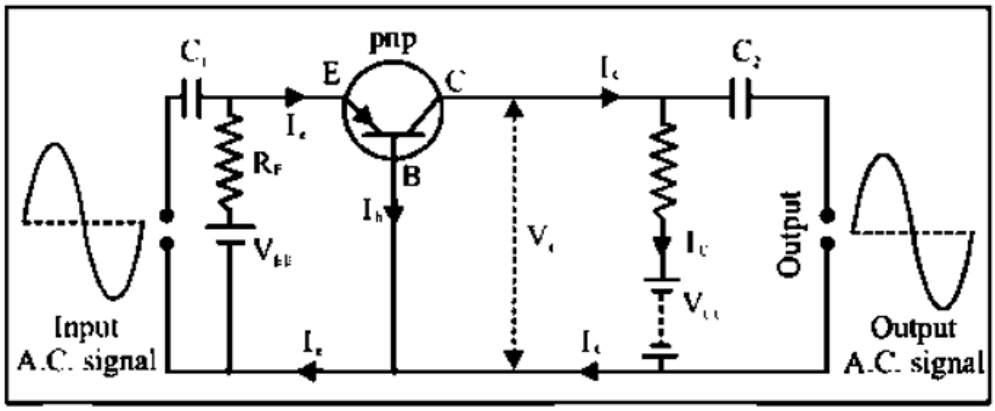
Low input voltage will be applied across emitter – base circuit and amplified circuit will be received across collector - base circuit. When I_e, I_b, I_c be the emitter, base and collector current then

$$I_e = I_b + I_c \ldots (i)$$

If current I_c is flowing in collector circuit, a potential drop I_cR_c will be happening the resistance connected in collector - base circuit and base collector voltage will be

$$V_{cb} = V_{cc} - I_cR_c ...(ii)$$

(b) Amplifier circuit by the use of p–n–p Transistor



1. If the positive half cycle of input a.c. signal voltage is coming, it supports the forward biasing of the emitter–base circuit. Due to this, the emitter current increases and consequently the collector current increases.
2. As I_c increases, the collector voltage V_c decreases.

3. Since the collector is connected to the negative terminal of V_{CC} battery of voltage V_{CB}, therefore, the reduction in collector voltage shows that the collector is becoming less negative. This is representing that while positive half cycle of input a.c. signal voltage occurs, the output signal voltage at the collector will be also varying through the positive half cycle.

4. In the same way, when a negative half cycle of input a.c. signal voltage occurs, the output signal voltage at the collector also varies through the negative half cycle. Hence, the input signal voltage and the output collector voltage are in the same phase in common base transistor amplifier circuit.

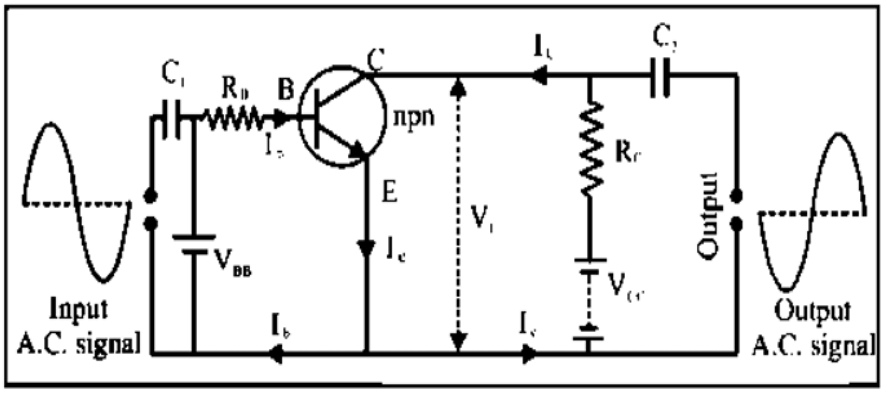
2.10 Common Emitter Amplifier

Amplifier circuit by the use of n–p-n transistor

1. The input (emitter base) circuit will be forward biased with battery V_{BB} of voltage V_{EB}, and the output (collector-emitter) circuit will be reversed biased with battery V_{CC} of voltage V_{CE}. Because of this, the resistance of input circuit will be low and that of output circuit will be high. R_c will be a load resistance connected in collector circuit.

2. If a.c. signal voltage has not been applied to the input circuit but emitter base circuit being closed, assume that I_e, I_b and I_c be the emitter current, base current and collector current respectively. Then in accordance to Kirchhoff's first law

$$I_e = I_b + I_c$$



If the positive half cycle of input a.c. signal voltage is considered, it will be supporting the forward biasing of the emitter-base circuit. Because of this, the emitter current will be increasing and as a result the collector

current will get increased. Because of which, the collector voltage V_c will be decreased.

3. Since the collector has been connected to the positive terminal of V_{CE} battery, therefore the reduction in voltage at the collector means the collector will become less positive, which shows that negative in accordance to initial value. This shows that while positive half cycle of input a.c. signal voltage occurs, the output signal voltage at the collector will be varying through a negative half cycle.

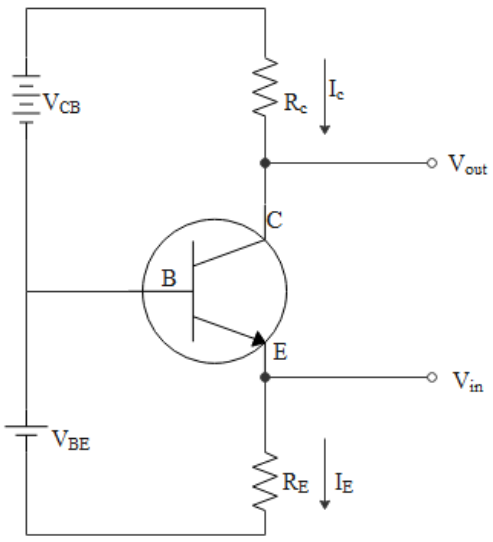
4. If negative half cycle of input a.c. signal voltage is considered, it will be opposing the forward biasing of emitter-base circuit, because of this the emitter current will be decreasing and therefore collector current will get decreased; As a result, the collector voltage V_c gets increased. That is, the collector will be more positive. This shows that when the negative half cycle of input a.c. signal voltage occurs, the output signal voltage will be varying through positive half cycle.

2.11 Common base Amplifier

A.c. current gain: This can be explained as the ratio of variation in collector current as fixed collector voltage. It is represented by α_{ac}.

$$\alpha_{ac} = \left(\frac{\Delta I_c}{\Delta I_e}\right)$$

$$[V_{CB} = \text{ const.}]$$



Voltage gain: This can be referred as the ratio of variation in output voltage to the variation in input voltage. It can be represented as A.

$$A_v = \frac{(\Delta I_c) R_{out}}{(\Delta I_e) R_{in}} = \frac{\Delta I_c}{\Delta I_e} \times \frac{R_{out}}{R_{in}}$$

Or $A_v = \alpha_{AC} \times$ resistance gain,

Where $\frac{R_{out}}{R_{in}}$ can be referred as resistance gain.

Power gain: This can be explained as the ratio of variation in output power to the variation in input power. Hence,

$$\text{a.c. power gain} = \frac{\text{change in output power}}{\text{change in input power}} = \frac{(\Delta I_c) R_{out}}{(\Delta I_e) R_{in}}$$

$$= \frac{\Delta I_c^2}{\Delta I_e^2} \times \frac{R_{out}}{R_{in}}$$

Or a.c. power gain $= \alpha_{ac}^2 \times$ resistance gain

2.12 Common Emitter Amplifier

A.c. current gain: The ratio of the variation in collector to the variation in base current can be defined as a.c current gain. It is represented as β_{ac}.

Hence,

$$\beta_{ac} = \left(\frac{\Delta I_c}{\Delta I_b} \right) \quad [V_{ce} = \text{ const.}]$$

The value of this quantity is quite large as compared to 1 and it lies between 15 to 50.

Voltage gain: The ratio of the variation in output voltage to the variation in input voltage can be referred as voltage gain. It is represented as A

$$A_v = \frac{(\Delta I_c) \times R_{out}}{(\Delta I_b) \times R_{in}} = \frac{\Delta I_c}{\Delta I_b} \times \frac{R_{out}}{R_{in}}$$

Or $A_v = \beta_{ac} \times$ resistance gain.

A.c. power gain: The ratio of the variation in output power to the variation in input power can be defined as A.c power gain.

$$\text{a.c. power gain}=\frac{\text{change in output power}}{\text{change in input power}}=\frac{(\Delta I_c)R_{out}}{(\Delta I_b)R_{in}}$$

Or a.c. power gain $=\beta^2_{ac}\times$ resistance gain .

2.13 Relation between α and β

In the case of both the types of amplifier, we will be having

$i_e = i_b + i_c$

Divide both sides of the equation given above by I_c, we will obtain,

$$\frac{i_e}{i_c}=\frac{i_b}{i_c}+1$$

$$\therefore \frac{1}{\alpha}=(\frac{1}{\beta})+1 \text{ or } \frac{1}{\beta}=(\frac{1}{\alpha})-1=\frac{(1-\alpha)}{\alpha}$$

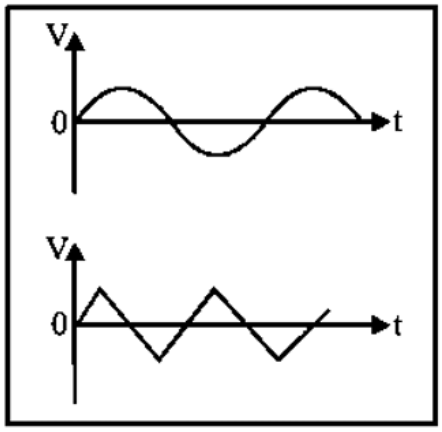
Or $\beta=\frac{\alpha}{(1-\alpha)}$

Similarly, The relation of α in terms of β ,

$$\alpha=\frac{\beta}{1+\beta}$$

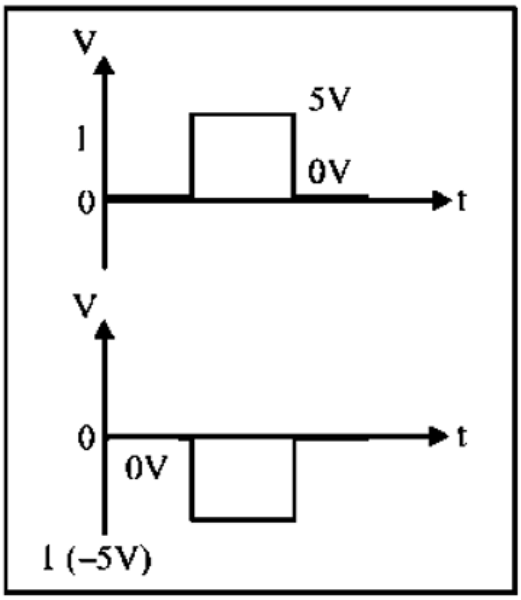
3. ANALOG SIGNALS

Analog signal can be defined as the signals which is varying continuously with respect to time. A typical analog signal has been represented in the diagram below. Circuit which has been used for the generation of analog signal can be defined as the analog electronic circuit.



4. DIGITAL SIGNALS

Signals which are having either of the two levels, 0 or 1, can be defined as digital signals.



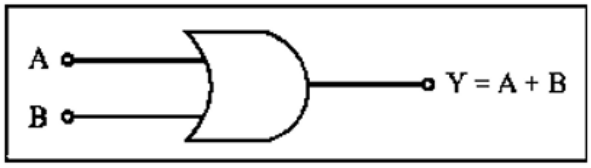
5. LOGIC GATES

A gate can be explained such that a digital circuit which is either stopping a signal or permitting it to pass through it. A logic gate will be an electronic circuit which will be creating logical decisions. Logic gate will be having one or more inputs but only one output. Logic gates are considered as the basic building blocks for every digital systems. Variables used at the input and output will be 1's and 0's. The three basic logic gates are mentioned below:

(i) OR gate
(ii) AND gate
(iii) NOT gate

5.1 OR Gate

OR gate can be considered as an electronic equipment that is combining A and B for ptoviding Y as output. Two inputs are A and B and output is Y in this figure. In Boolean algebra OR is shown as +.

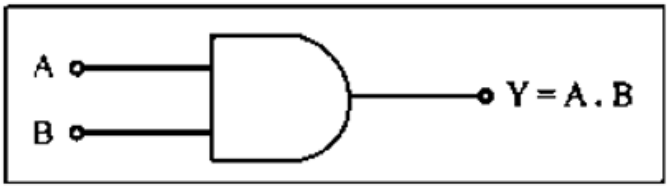


Truth Table: This can be defined as a table which is providing an output state for all possible input combinations.
Logic operations of OR gate has been provided in its truth table for all possible input combinations.

Input		Output
A	**B**	**Y**
0	0	0
0	1	1
1	0	1
1	1	1

5.2 AND Gate

There are two or more inputs and one output in an AND gate. In Boolean algebra AND has been denoted as a dot (.).

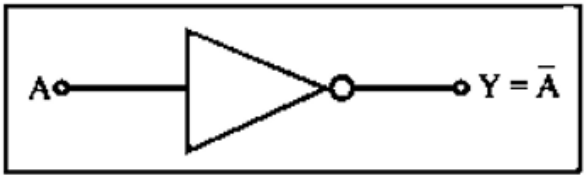


Truth Table

Input		Output
A	**B**	**Y**
0	0	0
0	1	0
1	0	0
1	1	1

5.3 NOT Gate

NOT gate can be considered as an electronic device which is having one input and one output. This circuit will be known as the same as the output is NOT the similar one as input.



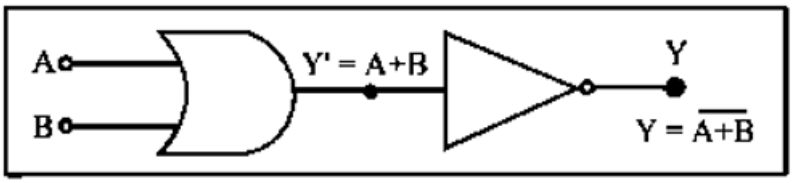
Boolean expression for NOT gate is $Y = \overline{A}$.

Truth Table:

Input	Out put
A	**Y**
0	1
1	0

5.4 NOR Gate

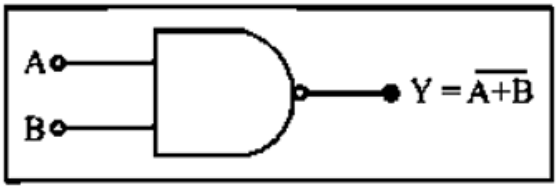
A NOR gate will be having two or more inputs and only one output. Here, NOR gate is a NOT-OR gate actually. When a NOT gate has been connected at the output of an OR gate, we will be getting NOR gate as represented in the diagram below and its truth table in table.



Truth Table:

A	B	Y′	Y
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

Boolean expression for NOT gate will be $Y = \overline{A + B}$ and this can be read as Y equals A OR B negated. A NOR function will be the reverse of OR function.



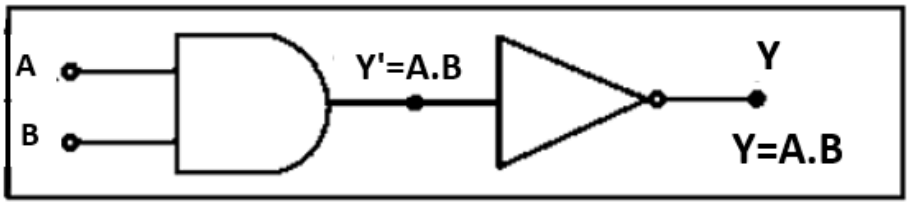
Truth Table:

Input		Output
A	**B**	**Y**
0	0	1
0	1	0

1	0	0
1	1	0

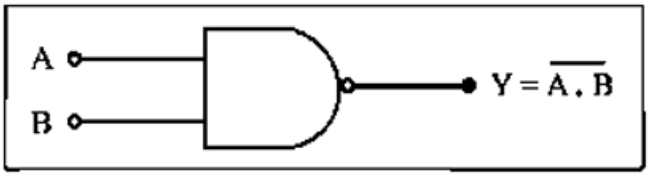
5.5 NAND Gate

A NAND gate will be having two or more inputs and only one output. A NAND gate is actually a NOT–AND gate. When a NOT gate has been connected at the output of a AND gate, we will be getting NAND gate as represented in the diagram and its truth table has been shown in table.



A	**B**	**Y′**	**Y**
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

Boolean expression for NAND gate, will be $Y = \overline{A \cdot B}$ and is read as Y equals A and B negated. Logical symbol of NAND gate has been represented in the diagram and its truth table in table.



Truth Table:

Input		**Output**
A	**B**	**Y**
0	0	1
0	1	1
1	0	1
1	1	0

Similar to NOR gate, NAND gate will also be useful to realize all basic gates: OR, AND and NOT. Therefore it is also called as **Universal Gate**.

Universal Gate:

A universal gate can be defined as a logic gate which can be used to perform any Boolean function with no utilization of any other type of logic gate. Examples of universal gates are NOR gate and NAND gate.

Integrated circuits:

The conventional process of creating circuits will be to choose components such as transistor, diodes, R, L, C etc., and connect them using soldering wires in the required manner. The commonly used technology will be the Monolithic Integrated Circuit. These kind of circuits is contained of logic gates. When we depend upon the level of integration (that is, the number of circuit components or logic gates), the ICs can be defined as Small Scale Integration, SSI (logic gates < 10), Medium Scale Integration, MSI (logic gates < 100), Large Scale Integration, LSI (logic gates < 1000) and Very Large Scale Integration, VLSI (logic gates > 1000).